Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-4, 11-15 and 21-25, and amend claims 32 and 40 as follows:

Listing of Claims:

1-31. (Canceled)

32. (Currently Amended) A method for writing data to a memory location in a memory system coupled to a bidirectional memory bus transmitting both read and write data, comprising:

~~accessing read data in~~ issuing a read command to the memory system;

providing a write command and corresponding write data to the memory system on the bidirectional memory bus, after issuing the read command;

coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data to be returned on the bidirectional data bus after the write data is provided to the same and before the write data has been written;

coupling the read data to the bidirectional memory bus and providing the read data for reading;

coupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location.

33. (Original) The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. (Original) The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. (Original) The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. (Previously Presented) A method for executing memory commands in a memory system having a memory bus on which both read and write data can be coupled, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data for the write command to the memory bus of the memory system after issuing the read command;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. (Original) The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. (Original) The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. (Original) The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. (Currently Amended) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.